REMARKS

Claims 9, 11, 12 and 16-25 are pending in the present application, were examined, and stand rejected. In response, Claims 9, 20 and 23 are amended, no claims are cancelled and no claims are added. Applicant respectfully requests reconsideration of pending Claims 9, 11, 12 and 16-25 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claim Objections

The Examiner has objected to Claims 9, 20 and 23 for informalities.

II. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claim 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,778,179 issued to Lavelle et al. ("Lavelle"). Applicant respectfully traverses this rejection.

Regarding Claim 20, Claim 20 recites the following claim feature, which is neither disclosed nor suggested by Lavelle or the references of record:

> the memory module to receive a writeback command, the writeback command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device. (Emphasis added.)

According to the Examiner, the above-recited feature of Claim 20 is disclosed by Lavelle at col. 9, line 59 - col. 10, line 2, col. 8, line 49 - col. 9, line 29, col. 10, line 57 – col. 11, line 12 and 313 of FIG. 7. (*See*, pg. 3, ¶4 of the Office Action mailed October 3, 2005.) After having carefully reviewed the passages cited by the Examiner, as well as the entire specification of Lavelle, Applicant respectfully disagrees with the Examiner's contention.

According to the Examiner, the video buffer shift register disclosed by Lavelle anticipates the eviction buffer recited by Claim 20. As recited by Lavelle:

> In order to provide for a continuous stream of pixels at the video output, the two shift registers may alternate duty (i.e., one loading data while the other is outputting data). The outputs of the two shift registers may then

be combined to a single stream of video data by a multiplexer 314. (col. 9, line 64 – col. 10, line 2.) (Emphasis added.)

As further described by Lavelle:

> The 3D-RAM devices 310 may also receive requests for video which cause data to be internally transferred from the appropriate DRAM banks 311 to the shift registers 313. In the embodiment shown, the video streams from all 3D-RAM devices 310 in the array are combined into a single video stream through the use of a multiplexer 322. The output of the multiplexer 322 may then be delivered to the video output processor 24 described in more detail below. In other embodiments of the memory array 301, the video streams from each 3D-RAM may be connected in parallel to form a video bus. In this case, the shift registers 313 may be furnished with output enable controls, where the assertion of an output enable may cause the associated shift register 313 to place data on the video bus. (col. 10, line 66 – col. 11, line 12.) (Emphasis added.)

Based on the cited passages above, Applicant respectfully submits that the Examiner has improperly equated the two video buffers/shift registers 313 disclosed by Lavelle with the eviction buffer recited by Claim 20. As recited by Claim 20, a writeback command causes a previous line of data, evicted from the data cache and stored with the eviction buffer, to be written out of the eviction buffer to the memory device.

In contrast to the features recited by Claim 20, Lavelle discloses that the outputs of the two shift registers may be combined into a single stream of video data by a multiplexer 314, which is delivered to video output processor 24. In other words, the video buffer/shift registers 313, as disclosed by Lavelle, are used to output a stream of data to video output processor 24 for eventual display by, for example, display device 84 (FIG. 1). (*See*, supra.)

Applicant respectfully asserts that the Patent Office has failed to adequately set forth a *prima facie* rejection under 35 U.S.C. §102(b). As mandated by case law, "anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik v. American Hoist & Derrick* ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)* (emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. *Titanium Metals Corp. of American v. Banner* ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

Regarding the eviction of data from, for example, level two cache 312, as disclosed by Lavelle, Lavelle discloses the following in response to a cache miss from the level two cache 312:

> If the requested data is not found in the level two cache (i.e., a level two cache miss), then the memory request processor 335 may request a page fetch by asserting the appropriate memory control signals 302. In this case, an entire page of pixel data is read from the appropriate DRAM bank 311 and deposited in the associated level two cache 312. Once the page fetch is completed, then the block transfer and pixel cache requests 303 described above may be issued. (col. 10, lines 57-65.) (Emphasis added.)

As further described by Lavelle:

> In some embodiments, this level two cache may be configured as a write-through cache (i.e., as data is written to the cache, the data is also written through, directly to the DRAM). (col. 9, lines 9-12.) (Emphasis added.).

Based on the cited passages above, Applicant respectfully submits that Lavelle fails to include any disclosure or even suggest the storage of data evicted from the level two (L2) cache within an eviction buffer, as recited by Claim 20. Furthermore, as indicated by Lavelle, L2 cache 312 may be configured as a write-through cache. (*See*, supra.) As a result, L2 cache would not contain any victim data that would have to be written back to the 3D-RAM 310, as recited by Claim 20.

Therefore, for at least the reasons provided above, Applicant respectfully submits that the Examiner is prohibited from relying on Lavelle as an anticipatory reference, since Lavelle fails to exactly disclose each and every element recited by Claim 20; specifically, a memory module to write out data from an eviction buffer to a memory device in response to a received writeback command. Banner Titanium, supra. Consequently, Applicant respectfully submits that the single prior art reference disclosure of Lavelle fails to include the presence of each and every element recited by Claim 20 and arranged in Claim 20, as required to establish a *prima facie* case of anticipation. Lindemann, supra.

Accordingly, Applicant respectfully submits that Claim 20 is patentable over Lavelle. Id. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 20.

Regarding Claims 21 and 22, Claims 21 and 22, based on their dependency from Claim 20, are also patentable over Lavelle, as well as the references of record.

Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claims 21 and 22.

The Examiner has rejected Claim 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,829,682 issued to Kirihata et al. ("Kirihata"). Applicant respectfully traverses this rejection.

Regarding Claim 20, Claim 20 recites the following claim feature, which is neither disclosed nor suggested by Kirihata or the references of record:

> the memory module to receive a writeback command, the writeback command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device. (Emphasis added.)

According to the Examiner, the above-recited feature of Claim 20 is disclosed by Kirihata at col. 4, lines 40-55, FIGS. 3-4 and col. 8, line 31 – col. 9, line 2. (*See*, pg. 3, ¶6 of the Office Action mailed October 3, 2005.) After having carefully reviewed the passages cited by the Examiner, as well as the entire specification of Kirihata, Applicant respectfully disagrees with the Examiner's contention.

According to the Examiner, write buffer 314, as disclosed by Kirihata, anticipates the eviction buffer recited by Claim 20. As recited by Claim 20, a previous line of data evicted from the data cache and stored within the eviction buffer is written out of the eviction buffer to the memory device in response to a received writeback command.

Hence, to anticipate Claim 20, the Examiner would have to illustrate the disclosure within Kirihata of the writeback buffer 314 storing data evicted from SRAM 304 and the storage of such data from writeback buffer 314 to DRAM array 302. However, Kirihata is devoid of any such disclosure and hence, neither discloses nor suggests the storage of data evicted from SRAM 304 and stored within write buffer and the consequent storage of such data to DRAM array 302 in response to a writeback command.

As disclosed by Kirihata:

> However, if the address bits are not matched (Write MISS/Write Back), the data bits in the write buffer 314 are written to the SRAM 304, while transferring the previously stored data bits back to the corresponding DRAM array 302 (referred to hereinafter as Delayed Write Back). The TAG memory 308 should be updated for storing new data in the SRAM 304. Alternatively, without writing to the SRAM 304 and without updating the TAG memory 308, the data bits in the write buffer 314 may be directly written back to the

DRAM core as a write through (referred to hereinafter as Write Through). (col. 6, lines 49-59.) (Emphasis added.)

As further disclosed by Kirihata,

> the write data bits on the data bit input pins (DI) are placed in a write buffer 314. (col. 6, lines 31-32.) (Emphasis added.)

Based on the cited passages above, as indicated by the delayed writeback embodiment disclosed by Kirihata, data evicted from SRAM 304, according to data bits in the write buffer 314, are stored to the corresponding DRAM array 302. (*See*, col. 6, lines 49-53.) As further indicated as a write through embodiment, data bits in the write buffer 314 may be directly written back to the DRAM core as a write through. (*See*, col. 6, lines 55-59.)

Accordingly, based on the cited passages above, data to be written to the DRAM array is initially placed within write buffer 314 and stored from write buffer 314 to SRAM 304, causing a delayed write back of evicted data from SRAM 304 to the corresponding DRAM array 302 according to the delayed write back mode. (*See*, col. 6, lines 49-53.) In the alternative embodiment described by Kirihata, the data bits from write buffer 304 are written directly back to the DRAM core without writing to SRAM 304, according to the write through mode.

Applicant respectfully asserts that the Patent Office has failed to adequately set forth a *prima facie* rejection under 35 U.S.C. §102(b). Here, the disclosure in Kirihata, is expressly limited to a write buffer 314 for storing data to be written to a DRAM array 302, either directly or via SRAM 304. (*See*, col. 6, lines 31-32 and 49-59.) In contrast to the above-recited features of Claim 20, write buffer 314 is not used to store data evicted from SRAM 304.

Conversely, as disclosed by Kirihata, in response to eviction of data from SRAM 304, such evicted data is transferred to DRAM array 302 prior to being overwritten by data bits in write buffer 304 according to the delayed writeback mode disclosed by Kirihata. (*See*, col. 6, lines 49-53.) In the alternative embodiment disclosed by Kirihata, data within the write buffer 304 may be directly written to the DRAM core according to the write through mode disclosed by Kirihata. Therefore, based on either the delayed writeback mode, the write-through mode or any other disclosed embodiment of Kirihata, Kirihata fails to disclose or suggest a previous line of data evicted from the data cache and stored within the

eviction buffer to be written out of the eviction buffer to the memory device in response to a received writeback command, as recited by Claim 20.

Consequently, for at least the reasons described above, Applicant respectfully submits that the Examiner is prohibited from relying on Kirihata as an anticipatory reference since Kirihata fails to exactly disclose each and every element recited by Claim 20 and specifically, the functionality performed by the memory module in response to the writeback command to cause a previous line of data evicted from the data cache and stored within the eviction buffer to be written out of the eviction buffer to the memory device. Banner , Titanium, supra.

Consequently, Applicant respectfully submits that the Examiner fails to illustrate that the single prior art reference disclosure of Kirihata includes the presence of each and every element recited by Claim 20, as arranged in Claim 20, and required to establish a *prima facie* case of anticipation. Lindemann, supra.

Accordingly, for at least the reasons described above, Applicant respectfully submits that Claim 20 is patentable over Kirihata, as well as the references of record. Id. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(e) rejection of Claim 20.

Regarding Claims 21 and 22, Claims 21 and 22, based on their dependency from Claim 20 and for at least the reasons described above, are also patentable over Kirihata, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(e) rejection of Claims 21 and 22.

III. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 9, 11-12 and 16-25 under 35 U.S.C. §103(a) as being unpatentable over Kirihata in view of U.S. Patent No. 5,526,510 issued to Akkary et al. ("Akkary"). Applicant respectfully traverses this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142) For the

reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Regarding Claim 9, Claim 9 recites the following claim features, which are neither disclosed nor suggested by the combination of Kirihata in view of Akkary:

> a system memory coupled to the memory controller, the system memory including at least two memory modules, each memory module including
>
> at least one memory device, and
>
> a data cache coupled to an eviction buffer, both coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into the eviction buffer. (Emphasis added.)

Applicant respectfully submits that neither the combination of Kirihata in view of Akkary, or the references of record, disclose a system memory including at least two memory modules, each memory module including at least one memory device having a data cache and an eviction buffer, as recited by Claim 9.

As indicated above, Claim 9 recites a data cache and an eviction buffer per memory module of a system memory, which includes at least two memory modules. Conversely, the memory architecture 300, as disclosed by Kirihata, includes a single buffer, or SRAM array 304, and a single write buffer 314, which the Examiner has incorrectly equated to the eviction buffer recited by Claim 9. In other words, as illustrated with reference to FIG. 3 of Kirihata:

> For purposes of illustration only, the following description assumes a total of 265 DRAM arrays, each consisting of 32K cells. The 32K cells are each accessed by 256 wordlines (WLs) and 128 bitline (BL) pairs. The SRAM array 304 is organized similar to each DRAM array 302 (having 32 K cells accessed by 256 WLs and 128 BL pairs). (col. 4, lines 49-55.) (Emphasis added.)

As indicated by pg. 4, ¶4 of the Office Action mailed October 3, 2005, the Examiner has equated DRAM arrays 302 to both a memory module and a memory device, system memory including at least two memory modules (302, FIG. 3), each memory including at least one memory device, i.e., memory cells (302, FIG. 4).

Applicant respectfully submits that the DRAM arrays 302 cannot be both a memory module and a memory device. Assuming that each DRAM array 302 disclosed by Kirihata

is a memory module, as suggested by the Examiner, then each memory module does not include a separate data buffer, which the Examiner equates to SRAM 304 and a separate eviction buffer, which the Examiner incorrectly equates to write buffer 314, per memory module, as recited by Claim 9

Alternatively, if each DRAM array is a memory device, then such memory device cannot be both a memory device and a memory module. Based on this interpretation, the memory architecture 300, as disclosed by Kirihata and shown in FIG. 3, includes a single memory module having a plurality of memory devices 302. Conversely, Claim 9 recites a system memory including at least two memory modules. Applicant respectfully submits that the memory architecture 300, as disclosed by Kirihata and illustrated in FIG. 3, includes a single memory module having 256 DRAM arrays 302.

However, regardless of the interpretation, the memory architecture 300, as disclosed by Kirihata, fails to teach or suggest a system memory including at least two memory modules, with each memory module including at least one memory device and a data cache coupled to an eviction buffer, both coupled to the memory device, as recited by Claim 9.

Regarding the Examiner's citing of Akkary, as illustrated by FIG. 2 of Akkary, assuming, arguendo, that writeback buffer 322 teaches or suggests the eviction buffer recited by Claim 9, the various data cache banks each share one single eviction buffer, writeback buffer 322. Accordingly, Applicant respectfully submits that the combination of Kirihata in view of Akkary fails to teach or suggest each of the recited features of Claim 9.

As mandated by case law, to establish a *prima facie* case of obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Here, Applicant respectfully submits that the combination of Kirihata in view of Akkary teach or suggest all claim features recited by Claim 9, as required to establish a *prima facie* case of obviousness. Hence, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of anticipation since all claim features recited by Claim 9 are neither taught nor suggested by the prior art combination of Kirihata in view of Akkary. Id.

Furthermore, Applicant respectfully disagrees with the Examiner's contention that one of ordinary skill in the art would modify the write buffer 314 of Kirihata, as disclosed by

Akkary. For at least the reasons indicated above with regards to the Examiner's rejection of Claim 20 under 35 U.S.C. §102(e) as anticipated by Kirihata, the write buffer 314 disclosed by Kirihata, is used for writing data to a DRAM array 302 of memory architecture 300 disclosed by Kirihata. (*See*, col. 6, lines 31-32 and 49-59.)

Applicant respectfully submits that since the write buffer 314 disclosed by Kirihata is not used to store evicted data but is, in fact, used to store data that is to be written into one of the DRAM arrays 302 (*see*, col. 6, lines 31-32 and 49-59) modification of such write buffer 314 to store data evicted from SRAM 304 would strictly prohibit the delayed writeback mode disclosed by Kirihata. As disclosed by Kirihata, writeback mode is performed in response to a write miss where data bits in the write buffer 314 are written to SRAM 304, while transferring the previously stored data bits from SRAM 304 back to the corresponding DRAM array 302. (*See*, col. 6, lines 49-53.)

As mandated by case law, "if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). Here, storing data evicted from SRAM 304 within write buffer 314 would alter the principle of operation of Kirihata since such modification would result in SRAM 304 retaining evicted data and data to be written to DRAM array 302 once such data is written to SRAM 304 from write buffer 314 according to the delayed writeback mode. Hence, such a modification is prohibited. Id.

Moreover, as mandated by case law, "if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, and there is no suggestion or motivation to make the proposed modification." In re Gordon, 733 F2d. 900, 221 USPQ 1125 (Fed. Cir. 1984.) Here, Applicant respectfully submits that storing data evicted from SRAM 304 within write buffer 314 would render Kirihata unsatisfactory for its intended purpose of increasing the transfer speed or bandwidth of DRAM devices by requiring the additional step of storing data evicted from SRAM 304 within write buffer 314. (*See*, col. 1, lines 28-37.)

Therefore, Applicant respectfully submits that since the proposed modification of Kirihata in view of Akkary renders Kirihata unsatisfactory for its intended purpose of

increasing DRAM transfer speed/bandwidth, the Examiner fails to illustrate a suggestion or motivation for making the proposed modifications to render Claim 9 obvious in view of the combination of Kirihata in view of Akkary. Id. In addition, since the proposed modification suggested by the Examiner to store data evicted from SRAM 304 within write buffer 314 alters the principle of operation of Kirihata, the combined teachings of Kirihata in view of Akkary are insufficient to render Claim 9 *prima facie* obvious. In re Ratti, supra.

Therefore, for at least the reasons described above, Applicant respectfully submits that Claim 9 is patentable over the combination of Kirihata in view of Akkary. Id. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9.

Regarding Claims 11 and 12, Claims 11 and 12, based on their dependency from Claim 9, are also patentable over the combination of Kirihata in view of Akkary. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 11 and 12.

Regarding Claim 16, Claim 16 recites the following claim features, which are neither disclosed nor suggested by the combination of Kirihata in view of Akkary:

> an array of tag address storage locations; and
> a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory module of a system memory, the command sequencer and serializer to deliver a writeback command to the eviction buffer associated with the memory module, the writeback command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to a memory device of the memory module. (Emphasis added.)

As recited by Claim 16, issuance of the writeback command to the eviction buffer associated with the memory module causes the previous line of data evicted from the data cache and stored in the eviction buffer to be written out to a memory device of the memory module. Applicant respectfully disagrees with the Examiner's contention that one of ordinary skill in the art would modify the write buffer 314 of Kirihata, as disclosed by Akkary.

For at least the reasons indicated above with regards to the Examiner's rejection of Claim 20 under 35 U.S.C. §102(e) as anticipated by Kirihata, the write buffer 314 disclosed by Kirihata, is used for writing data to a DRAM array 302 of memory architecture 300 disclosed by Kirihata. (*See,* col. 6, lines 31-32 and 49-59.)

Applicant respectfully submits that since the write buffer 314 disclosed by Kirihata is not used to store evicted data but is, in fact, used to store data that is to be written into one of the DRAM arrays 302 (*see*, col. 6, lines 31-32 and 49-59) modification of such write buffer 314 to store data evicted from SRAM 304 would strictly prohibit the delayed writeback mode disclosed by Kirihata. As disclosed by Kirihata, writeback mode is performed in response to a write miss where data bits in the write buffer 314 are written to SRAM 304, while transferring the previously stored data bits from SRAM 304 back to the corresponding DRAM array 302. (*See*, col. 6, lines 49-53.)

Applicant respectfully submits that storing data evicted from SRAM 304 within write buffer 314 would alter the principle of operation of Kirihata since such modification would result in SRAM 304 retaining evicted data and data to be written to DRAM array 302 once such data is written to SRAM 304 from write buffer 314 according to the delayed writeback mode. Hence, since the proposed modification changes the principle of operation of Kirihata, the teachings of Kirihata in view of Akkary are not sufficient to render Claim 16 *prima facie* obvious. In re Ratti, supra.

Moreover, Applicant respectfully submits that storing data evicted from SRAM 304 within write buffer 314 would render Kirihata unsatisfactory for its intended purpose of increasing the transfer speed or bandwidth of DRAM devices by requiring the additional step of storing data evicted from SRAM 304 within write buffer 314. (*See*, col. 1, lines 28-37.) Hence, since the proposed modification would render Kirihata unsatisfactory for its intended purpose, there is no suggestion or motivation to make the proposed modification. In re Gordon, supra.

Therefore, Applicant respectfully submits that since the proposed modification of Kirihata in view of Akkary renders Kirihata unsatisfactory for its intended purpose of increasing DRAM transfer speed/bandwidth, the Examiner fails to illustrate a suggestion or motivation for making the proposed modifications to render Claim 16 obvious in view of the combination of Kirihata in view of Akkary. Id. In addition, since the proposed modification suggested by the Examiner to store data evicted from SRAM 304 within write buffer 314 alters the principle of operation of Kirihata, the combined teachings of Kirihata in view of Akkary are insufficient to render Claim 16 *prima facie* obvious. In re Ratti, supra.

Consequently, for at least the reasons described above, Claim 16 is patentable over the combination of Kirihata in view of Akkary. Id. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 16.

Regarding Claims 17-19, Claims 17-19, based on their dependency from Claim 16, are also patentable over the combination of Kirihata in view of Akkary. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

Regarding Claim 20, Applicant's arguments provided above with regard to Claim 16 regarding the issuance of a writeback command to cause the previous line of data evicted from the data cache and stored within the eviction buffer to be written out of the eviction buffer to a memory device apply to the Examiner's rejection of Claim 20 under 35 U.S.C. §103(a) as being unpatentable over Kirihata in view Akkary, since Claim 20 recites an analogous claim feature.

As indicated above regarding the Examiner's rejection of Claim 16 under 35 U.S.C. §103(a) as being unpatentable over Kirihata in view Akkary, the proposed modification of Kirihata in view of Akkary renders Kirihata unsatisfactory for its intended purpose of increasing DRAM transfer speed/bandwidth. Consequently, the Examiner fails to illustrate a suggestion or motivation for making the proposed modifications to render Claim 20 obvious in view of the combination of Kirihata in view of Akkary. In re Gordon, supra.

In addition, since the proposed modification suggested by the Examiner to store data evicted from SRAM 304 within write buffer 314 alters the principle of operation of Kirihata, the combined teachings of Kirihata in view of Akkary are insufficient to render Claim 20 *prima facie* obvious. In re Ratti, supra.

Accordingly, for at least the reasons described above, Applicant respectfully submits that Claim 20 is patentable over the combination of Hirikata in view of Akkary. Id. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 20.

Regarding Claims 21 and 22, Claims 21 and 22, based on their dependency from Claim 20, are also patentable over the combination of Hirikata in view of Akkary. Id.

Regarding Claim 23, for at least the reasons provided above with regard to Claim 9, based on the first interpretation of the Examiner's rejection of Claim 9, Hirikata neither discloses a single memory module, which includes at least one memory device, and a data cache coupled to a write buffer (and not an eviction buffer, as recited by Claim 23), both coupled to the memory device. According to the alternative interpretation where each memory array 302, as disclosed by Hirikata, represents a single memory module, such memory modules do not each include a separate data cache and eviction buffer, as recited by Claim 23.

Consequently, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness, since establishing a *prima facie* case of obviousness of a claimed invention requires that all claim limitations must be taught or suggested by the prior art. In re Royka, supra. Here, Hirikata fails to disclose each of the recited features of Claim 23, including at least two memory modules, each memory module including at least one memory device, in a data cache coupled to an eviction buffer, both coupled to the memory device, as required to establish a *prima facie* case of obviousness. Id.

Consequently, Claim 23 is patentable over the combination of Hirikata in view of Akkary. Id. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 23.

Regarding Claims 24 and 25, Claims 24 and 25, based on their dependency from Claim 23, are also patentable over the combination of Hirikata in view of Akkary. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 24 and 25.

CONCLUSION

In view of the foregoing, it is submitted that Claims 9, 11 12 and 16-25, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: January 3, 2006

By: _____
Joseph Lutz, Reg. No. 43,765

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 3, 2006

Marilyn Bass January 3, 2006